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**JK Lakshmipat University**

[**Computer**](https://canvas.instructure.com/courses/8496533) **Organization and Architecture**

**ASSIGNMENT 2**

**Name – Indrajit Roy**

**Section – B**

**Roll No.- 2023BTECH037**

**Date of Submission – 15th October, 2024**

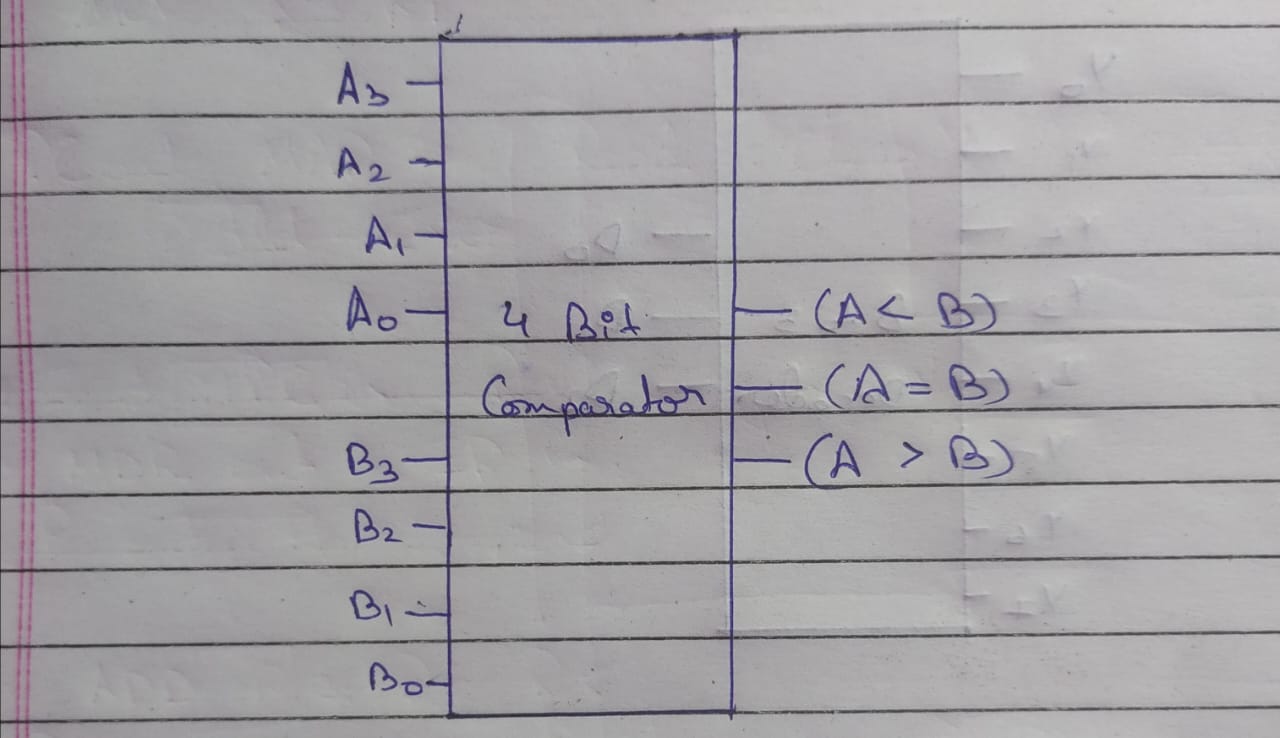
**Submitted To – DR. Pranab Roy Sir**

**Question 1**

**Design a VHDL model for a hardwired 4-Bit comparator using dataflow architecture**

**Aim : To Design and implement a 4-bit comparator using the data flow architecture in VHDL  to compare two 4-bit binary numbers (A and B) and to produce an output telling whether A is equal to, greater than, or less than B.**

**Block Diagram :**



***● VHDL Code:***

***----------------------------------------------------------------------------------***

***-- Company:***

***-- Engineer:***

***-- Create Date: 19:32:16 09/22/2024***

***-- Design Name:***

***-- Module Name: comparator - Behavioral***

***-- Project Name:***

***-- Target Devices:***

***-- Tool versions:***

***-- Description:***

***-- Dependencies:***

***-- Revision:***

***-- Revision 0.01 - File Created***

***-- Additional Comments:***

***---------------------------------------------------------------------------------***

***library IEEE;***

***use IEEE.STD\_LOGIC\_1164.ALL;***

***-- Uncomment the following library declaration if using***

***-- arithmetic functions with Signed or Unsigned values***

***--use IEEE.NUMERIC\_STD.ALL;***

***-- Uncomment the following library declaration if instantiating***

***-- any Xilinx primitives in this code.***

***--library UNISIM;***

***--use UNISIM.VComponents.all;***

***entity comparator is***

***PORT(***

***A,B:IN STD\_LOGIC\_VECTOR(3 DOWNTO 0);***

***g,l,e: out std\_logic);***

***end comparator;***

***architecture Behavioral of comparator is***

***signal s:std\_logic\_vector (3 downto 0);***

***begin***

***s(0)<=A(0) XNOR B(0);***

***s(1)<=A(1) XNOR B(1);***

***s(2)<=A(2) xNor B(2);***

***s(3)<=A(3) XNOR B(3);***

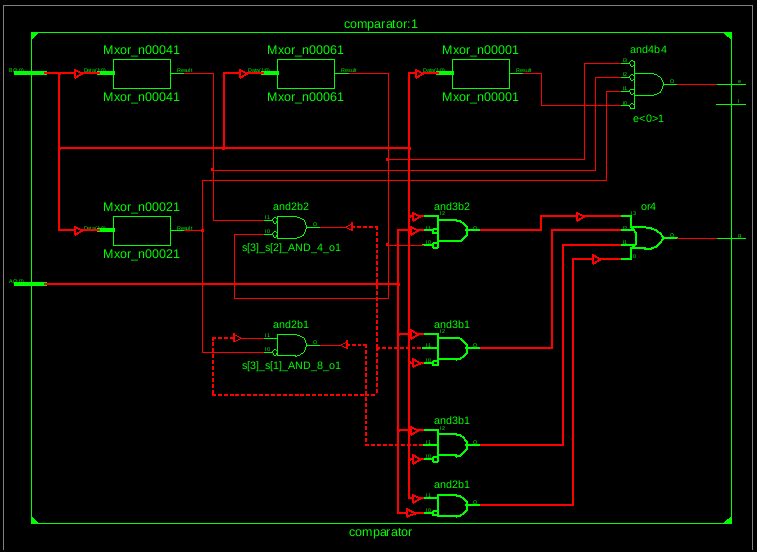
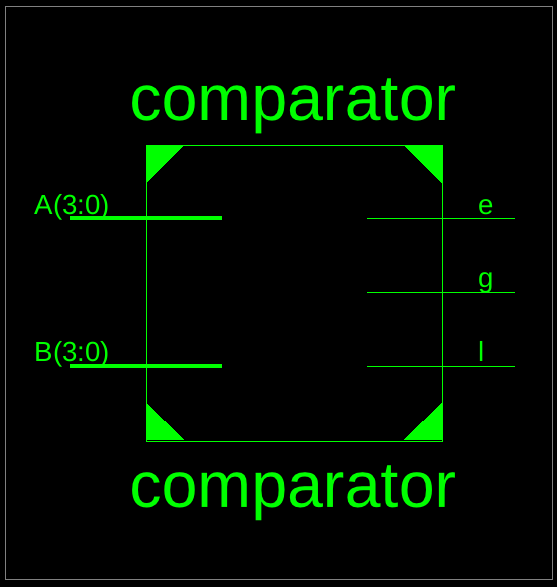
***g<=(A(3) AND NOT (B(3))) OR (s(3) and (A(2) AND (NOT B(2)))) OR(s(3) and s(2) and (A(1) AND (NOT (B(1))))) OR (s(3) and s(2) and s(1) and (A(0) AND (NOT B(0))));***

***l<=(NOT(A(3)) AND B(3)) OR (s(3) and (NOT(A(2)) AND B(2))) OR(s(3) and s(2) and (NOT (A(1)) AND (B(1)))) OR (s(3) and s(2) and s(1) and (NOT(A(0)) AND B(0)));***

***e<=(s(0) and s(1) and s(2) and s(3));***

***end Behavioral;***

***● RTL Diagram:***



***● Testbench Code:***

***--------------------------------------------------------------------------------***

***-- Company:***

***-- Engineer:***

***--***

***-- Create Date: 19:40:53 09/22/2024***

***-- Design Name:***

***-- Module Name: /home/ise/Assignment2/tb\_comparator.vhd***

***-- Project Name: Assignment2***

***-- Target Device:***

***-- Tool versions:***

***-- Description:***

***--***

***-- VHDL Test Bench Created by ISE for module: comparator***

***--***

***-- Dependencies:***

***--***

***-- Revision:***

***-- Revision 0.01 - File Created***

***-- Additional Comments:***

***--***

***-- Notes:***

***-- This testbench has been automatically generated using types std\_logic and***

***-- std\_logic\_vector for the ports of the unit under test. Xilinx recommends***

***-- that these types always be used for the top-level I/O of a design in order***

***-- to guarantee that the testbench will bind correctly to the post-implementation***

***-- simulation model.***

***--------------------------------------------------------------------------------***

***LIBRARY ieee;***

***USE ieee.std\_logic\_1164.ALL;***

***-- Uncomment the following library declaration if using***

***-- arithmetic functions with Signed or Unsigned values***

***--USE ieee.numeric\_std.ALL;***

***ENTITY tb\_comparator IS***

***END tb\_comparator;***

***ARCHITECTURE behavior OF tb\_comparator IS***

***-- Component Declaration for the Unit Under Test (UUT)***

***COMPONENT comparator***

***PORT(***

***A : IN std\_logic\_vector(3 downto 0);***

***B : IN std\_logic\_vector(3 downto 0);***

***g : OUT std\_logic;***

***l : OUT std\_logic;***

***e : OUT std\_logic***

***);***

***END COMPONENT;***

***--Inputs***

***signal A : std\_logic\_vector(3 downto 0) := (others => '0');***

***signal B : std\_logic\_vector(3 downto 0) := (others => '0');***

***--Outputs***

***signal g : std\_logic;***

***signal l : std\_logic;***

***signal e : std\_logic;***

***-- No clocks detected in port list. Replace <clock> below with***

***-- appropriate port name***

***BEGIN***

***-- Instantiate the Unit Under Test (UUT)***

***uut: comparator PORT MAP (***

***A => A,***

***B => B,***

***g => g,***

***l => l,***

***e => e***

***);***

***-- Stimulus process***

***stim\_proc: process***

***begin***

***A <= "1001"; B <= "1000";***

***wait for 100 ns;***

***A <= "1101"; B <= "1101";***

***wait for 100 ns;***

***A <= "0000"; B <= "0001";***

***wait for 100 ns;***

***A <= "0000"; B <= "0000";***

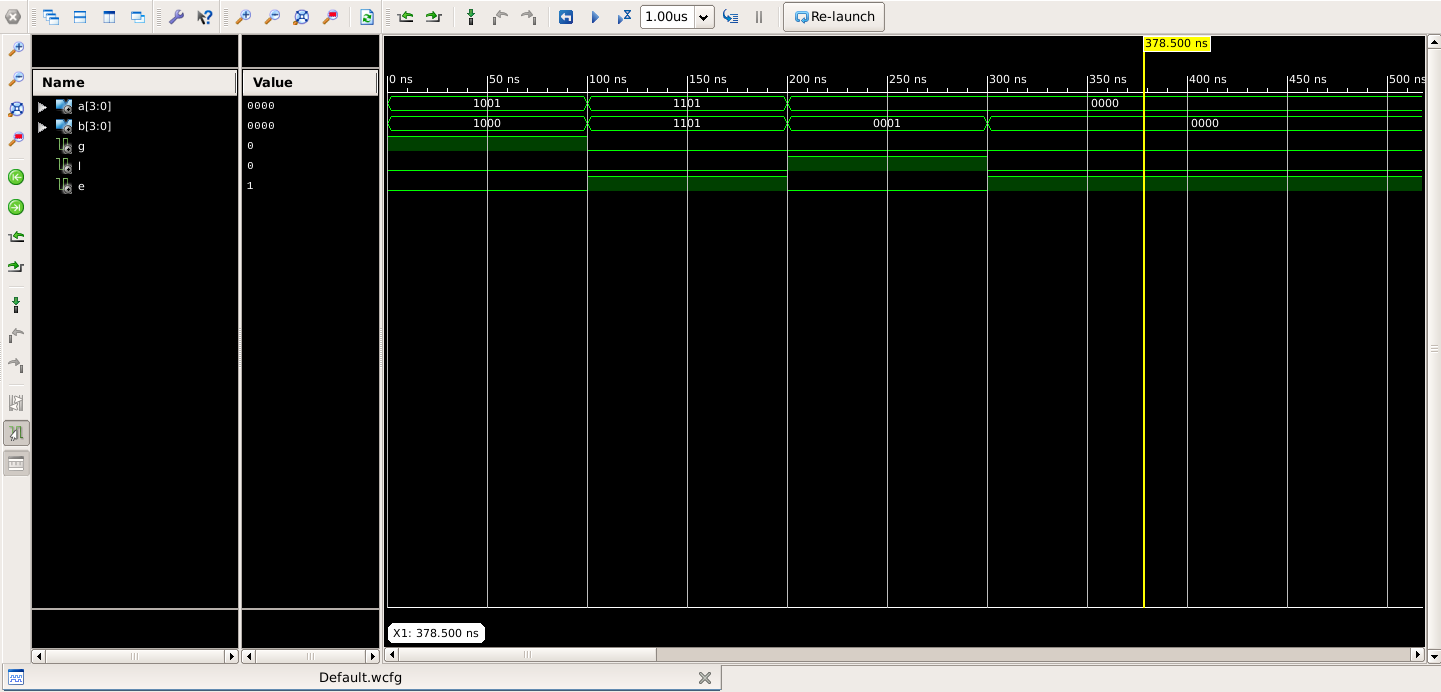
***wait for 100 ns;***

***wait;***

***end process;***

***END;***

***● Waveform:***

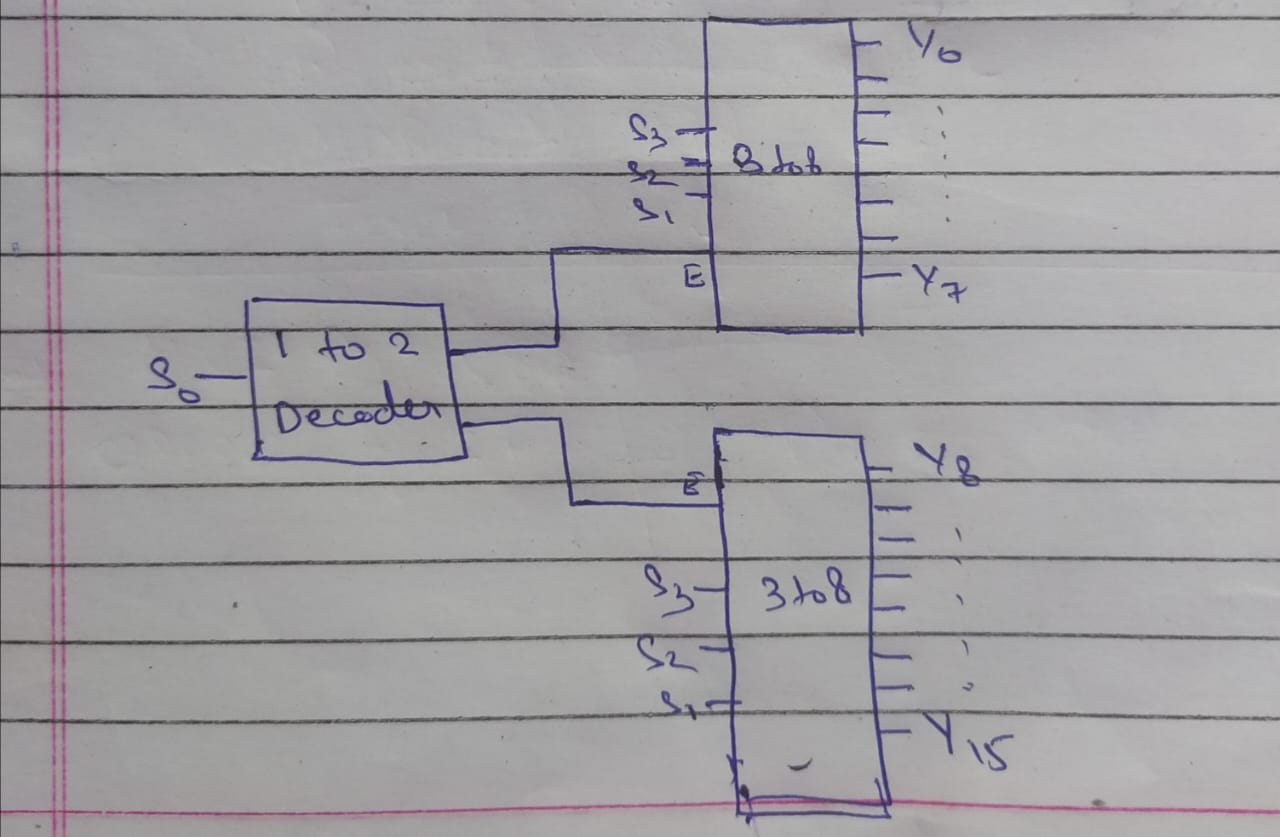
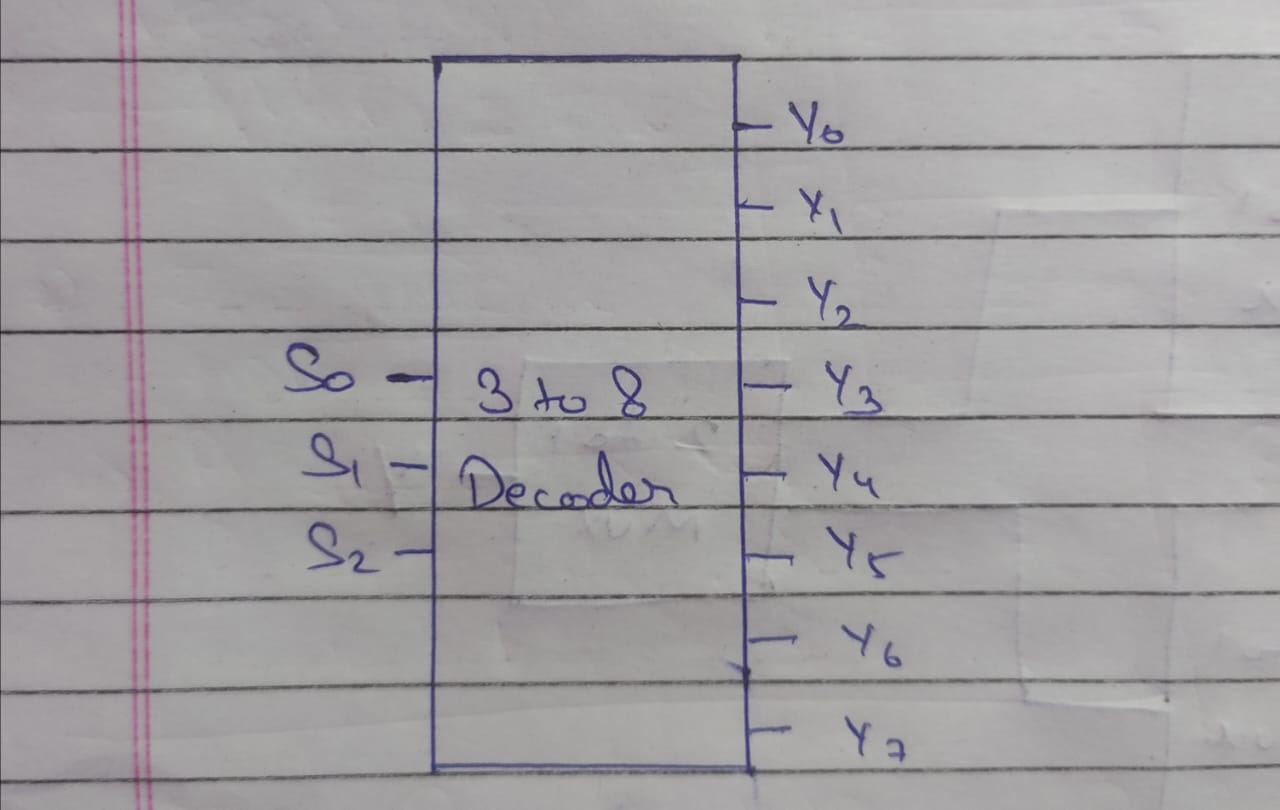


**Question 2**

**Design a VHDL model for a 3 to 8 Decoder (with an enable) using Dataflow Architecture. Thereby Design a VHDL model for a 4 to 16 Decoder using 3 to 8 decoders designed earlier using Structural Architecture**

**Aim : To design a 3-to-8 Decoder with an enable signal using Dataflow Architecture and then use the designed 3-to-8 Decoder to create a 4-to-16 Decoder using Structural Architecture in VHDL.**

**Circuit Diagram :**



**3 to 8 Decoder:**

***● VHDL Code:***

***----------------------------------------------------------------------------------***

***-- Company:***

***-- Engineer:***

***--***

***-- Create Date: 19:49:45 09/22/2024***

***-- Design Name:***

***-- Module Name: decoder\_3\_to\_8 - Behavioral***

***-- Project Name:***

***-- Target Devices:***

***-- Tool versions:***

***-- Description:***

***--***

***-- Dependencies:***

***--***

***-- Revision:***

***-- Revision 0.01 - File Created***

***-- Additional Comments:***

***--***

***----------------------------------------------------------------------------------***

***library IEEE;***

***use IEEE.STD\_LOGIC\_1164.ALL;***

***-- Uncomment the following library declaration if using***

***-- arithmetic functions with Signed or Unsigned values***

***--use IEEE.NUMERIC\_STD.ALL;***

***-- Uncomment the following library declaration if instantiating***

***-- any Xilinx primitives in this code.***

***--library UNISIM;***

***--use UNISIM.VComponents.all;***

***entity decoder\_3\_to\_8 is***

***Port ( A : in STD\_LOGIC\_VECTOR (2 DOWNTO 0);***

***E : in STD\_LOGIC;***

***Y : out STD\_LOGIC\_VECTOR (7 DOWNTO 0));***

***end decoder\_3\_to\_8;***

***architecture Behavioral of decoder\_3\_to\_8 is***

***begin***

***Y(0) <= (NOT A(0)) AND (NOT A(1)) AND (NOT A(2)) AND E;***

***Y(1) <= (NOT A(0)) AND (NOT A(1)) AND A(2) AND E;***

***Y(2) <= (NOT A(0)) AND A(1) AND (NOT A(2)) AND E;***

***Y(3) <= (NOT A(0)) AND A(1) AND A(2) AND E;***

***Y(4) <= A(0) AND (NOT A(1)) AND (NOT A(2)) AND E;***

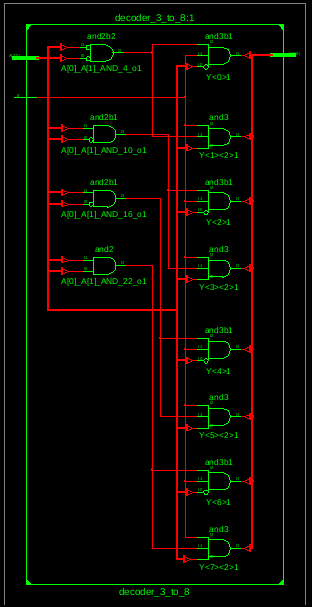
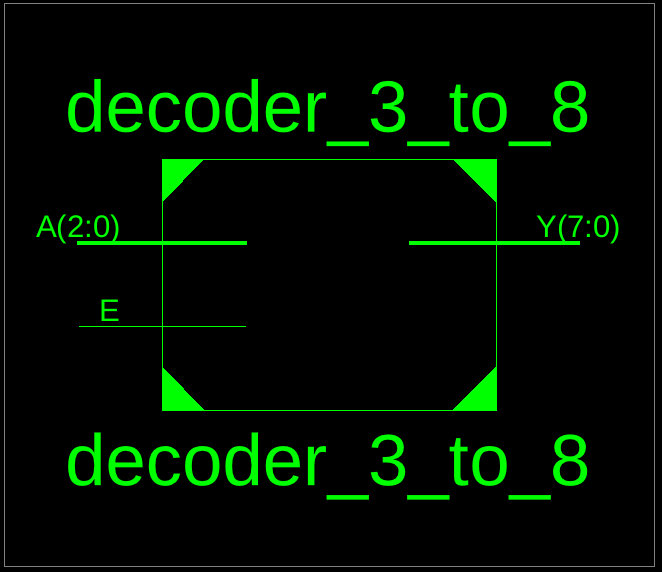
***Y(5) <= A(0) AND (NOT A(1)) AND A(2) AND E;***

***Y(6) <= A(0) AND A(1) AND (NOT A(2)) AND E;***

***Y(7) <= A(0) AND A(1) AND A(2) AND E;***

***end Behavioral;***

***● RTL Diagram:***



***● Testbench Code:***

***--------------------------------------------------------------------------------***

***-- Company:***

***-- Engineer:***

***--***

***-- Create Date: 19:55:19 09/22/2024***

***-- Design Name:***

***-- Module Name: /home/ise/Assignment2/tb\_decoder\_3\_to\_8.vhd***

***-- Project Name: Assignment2***

***-- Target Device:***

***-- Tool versions:***

***-- Description:***

***--***

***-- VHDL Test Bench Created by ISE for module: decoder\_3\_to\_8***

***--***

***-- Dependencies:***

***--***

***-- Revision:***

***-- Revision 0.01 - File Created***

***-- Additional Comments:***

***--***

***-- Notes:***

***-- This testbench has been automatically generated using types std\_logic and***

***-- std\_logic\_vector for the ports of the unit under test. Xilinx recommends***

***-- that these types always be used for the top-level I/O of a design in order***

***-- to guarantee that the testbench will bind correctly to the post-implementation***

***-- simulation model.***

***--------------------------------------------------------------------------------***

***LIBRARY ieee;***

***USE ieee.std\_logic\_1164.ALL;***

***-- Uncomment the following library declaration if using***

***-- arithmetic functions with Signed or Unsigned values***

***--USE ieee.numeric\_std.ALL;***

***ENTITY tb\_decoder\_3\_to\_8 IS***

***END tb\_decoder\_3\_to\_8;***

***ARCHITECTURE behavior OF tb\_decoder\_3\_to\_8 IS***

***-- Component Declaration for the Unit Under Test (UUT)***

***COMPONENT decoder\_3\_to\_8***

***PORT(***

***A : IN std\_logic\_vector(2 downto 0);***

***E : IN std\_logic;***

***Y : OUT std\_logic\_vector(7 downto 0)***

***);***

***END COMPONENT;***

***--Inputs***

***signal A : std\_logic\_vector(2 downto 0) := (others => '0');***

***signal E : std\_logic := '0';***

***--Outputs***

***signal Y : std\_logic\_vector(7 downto 0);***

***-- No clocks detected in port list. Replace <clock> below with***

***-- appropriate port name***

***BEGIN***

***-- Instantiate the Unit Under Test (UUT)***

***uut: decoder\_3\_to\_8 PORT MAP (***

***A => A,***

***E => E,***

***Y => Y***

***);***

***-- Stimulus process***

***stim\_proc: process***

***begin***

***A <= "111";***

***E <= '1';***

***WAIT FOR 100 ns;***

***A <= "010";***

***E <= '1';***

***WAIT FOR 100 ns;***

***A <= "001";***

***E <= '1';***

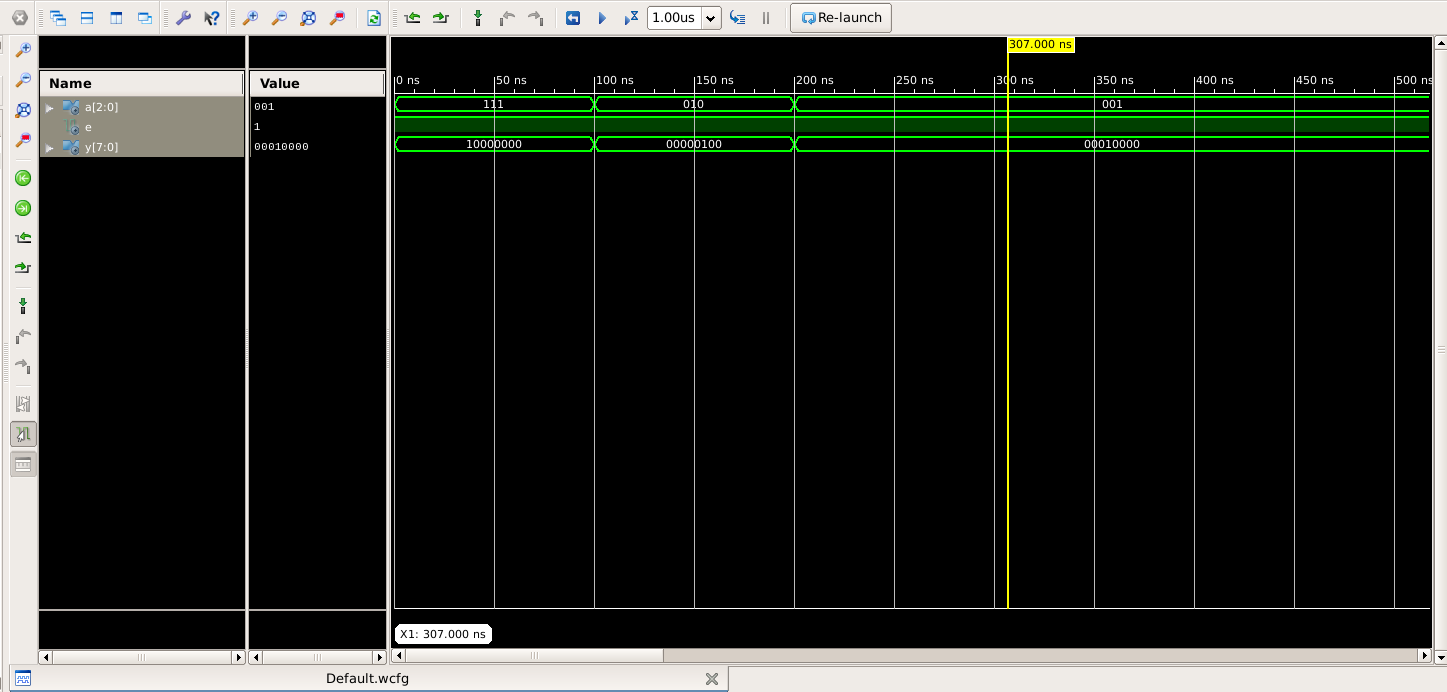
***WAIT FOR 100 ns;***

***wait;***

***end process;***

***END;***

***● Waveform:***



**4 to 16 Decoder:**

***● VHDL Code:***

***----------------------------------------------------------------------------------***

***-- Company:***

***-- Engineer:***

***--***

***-- Create Date: 20:00:13 09/22/2024***

***-- Design Name:***

***-- Module Name: decoder\_4\_to\_16 - Behavioral***

***-- Project Name:***

***-- Target Devices:***

***-- Tool versions:***

***-- Description:***

***--***

***-- Dependencies:***

***--***

***-- Revision:***

***-- Revision 0.01 - File Created***

***-- Additional Comments:***

***--***

***----------------------------------------------------------------------------------***

***library IEEE;***

***use IEEE.STD\_LOGIC\_1164.ALL;***

***-- Uncomment the following library declaration if using***

***-- arithmetic functions with Signed or Unsigned values***

***--use IEEE.NUMERIC\_STD.ALL;***

***-- Uncomment the following library declaration if instantiating***

***-- any Xilinx primitives in this code.***

***--library UNISIM;***

***--use UNISIM.VComponents.all;***

***entity decoder\_4\_to\_16 is***

***Port (***

***A : IN STD\_LOGIC\_VECTOR (3 DOWNTO 0);***

***E : in std\_logic;***

***Y : OUT STD\_LOGIC\_VECTOR (15 DOWNTO 0)***

***);***

***end decoder\_4\_to\_16;***

***architecture Behavioral of decoder\_4\_to\_16 is***

***COMPONENT decoder\_3\_to\_8 IS***

***Port (***

***A : IN STD\_LOGIC\_VECTOR (2 DOWNTO 0);***

***E : IN STD\_LOGIC;***

***Y : OUT STD\_LOGIC\_VECTOR (7 DOWNTO 0)***

***);***

***END COMPONENT;***

***component decoder\_1\_to\_2 is***

***Port ( Y : in STD\_LOGIC;***

***E : in STD\_LOGIC;***

***Y1 : out STD\_LOGIC;***

***Y2 : out STD\_LOGIC);***

***end component;***

***signal t1,t2: STD\_LOGIC;***

***begin***

***step1:decoder\_1\_to\_2 port map(A(0),E,t1,t2);***

***L1: decoder\_3\_to\_8 PORT MAP (***

***A=> A(2 downto 0),***

***E => t1,***

***Y(0) => Y(0),***

***Y(1) => Y(1),***

***Y(2) => Y(2),***

***Y(3) => Y(3),***

***Y(4) => Y(4),***

***Y(5) => Y(5),***

***Y(6) => Y(6),***

***Y(7) => Y(7)***

***);***

***L2: decoder\_3\_to\_8 PORT MAP (***

***A => A(2 DOWNTO 0),***

***E => t2,***

***Y(0) => Y(8),***

***Y(1) => Y(9),***

***Y(2) => Y(10),***

***Y(3) => Y(11),***

***Y(4) => Y(12),***

***Y(5) => Y(13),***

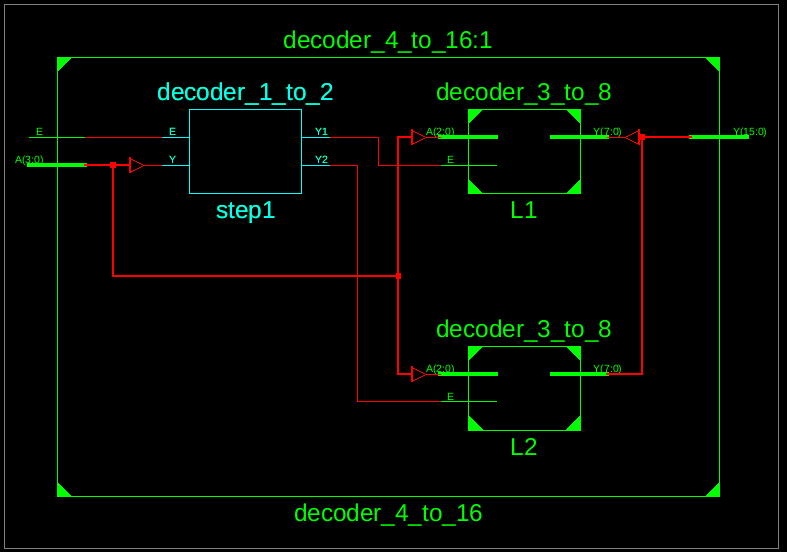
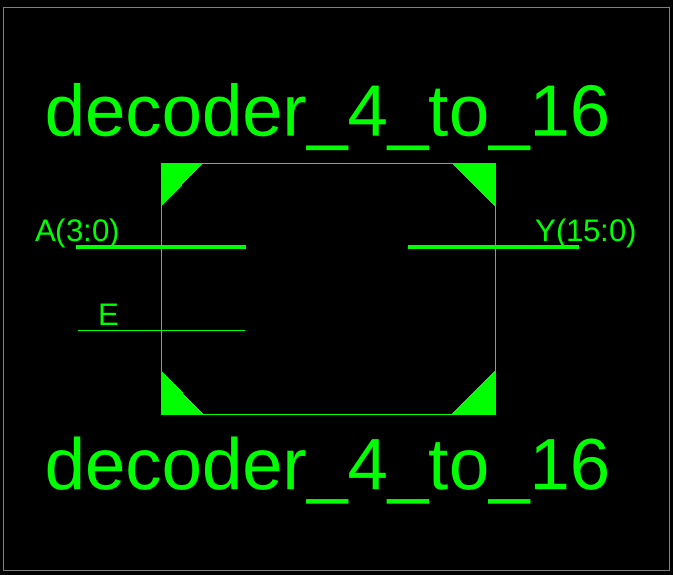
***Y(6) => Y(14),***

***Y(7) => Y(15)***

***);***

***end Behavioral;***

***● RTL Diagram:***



***● Testbench Code:***

***--------------------------------------------------------------------------------***

***-- Company:***

***-- Engineer:***

***--***

***-- Create Date: 20:07:40 09/22/2024***

***-- Design Name:***

***-- Module Name: /home/ise/Assignment2/tb\_decoder\_4\_to\_16.vhd***

***-- Project Name: Assignment2***

***-- Target Device:***

***-- Tool versions:***

***-- Description:***

***--***

***-- VHDL Test Bench Created by ISE for module: decoder\_4\_to\_16***

***--***

***-- Dependencies:***

***--***

***-- Revision:***

***-- Revision 0.01 - File Created***

***-- Additional Comments:***

***--***

***-- Notes:***

***-- This testbench has been automatically generated using types std\_logic and***

***-- std\_logic\_vector for the ports of the unit under test. Xilinx recommends***

***-- that these types always be used for the top-level I/O of a design in order***

***-- to guarantee that the testbench will bind correctly to the post-implementation***

***-- simulation model.***

***--------------------------------------------------------------------------------***

***LIBRARY ieee;***

***USE ieee.std\_logic\_1164.ALL;***

***-- Uncomment the following library declaration if using***

***-- arithmetic functions with Signed or Unsigned values***

***--USE ieee.numeric\_std.ALL;***

***ENTITY tb\_decoder\_4\_to\_16 IS***

***END tb\_decoder\_4\_to\_16;***

***ARCHITECTURE behavior OF tb\_decoder\_4\_to\_16 IS***

***-- Component Declaration for the Unit Under Test (UUT)***

***COMPONENT decoder\_4\_to\_16***

***PORT(***

***A : IN std\_logic\_vector(3 downto 0);***

***E : IN std\_logic;***

***Y : OUT std\_logic\_vector(15 downto 0)***

***);***

***END COMPONENT;***

***--Inputs***

***signal A : std\_logic\_vector(3 downto 0) := (others => '0');***

***signal E : std\_logic := '0';***

***--Outputs***

***signal Y : std\_logic\_vector(15 downto 0);***

***-- No clocks detected in port list. Replace <clock> below with***

***-- appropriate port name***

***BEGIN***

***-- Instantiate the Unit Under Test (UUT)***

***uut: decoder\_4\_to\_16 PORT MAP (***

***A => A,***

***E => E,***

***Y => Y***

***);***

***-- Stimulus process***

***stim\_proc: process***

***begin***

***E<='1';***

***A<="1111";***

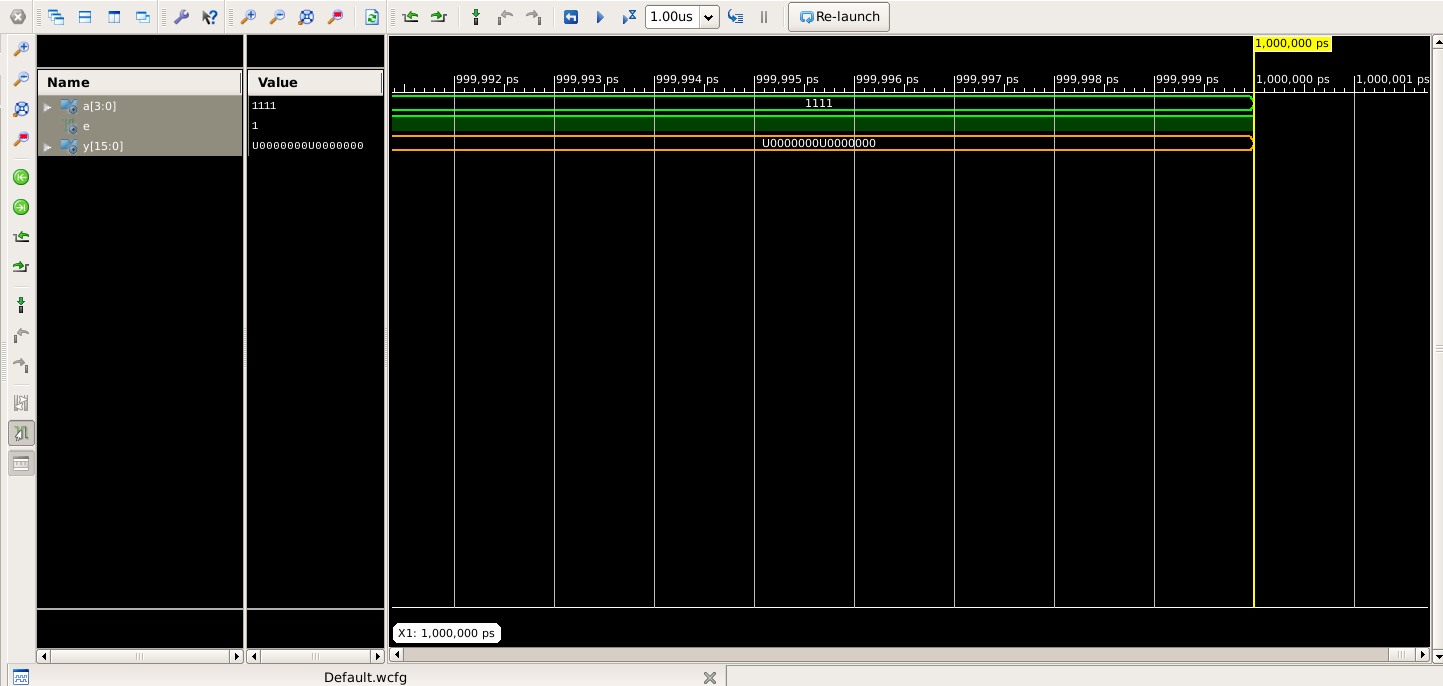
***wait for 100 ns;***

***wait;***

***end process;***

***END;***

***● Waveform:***

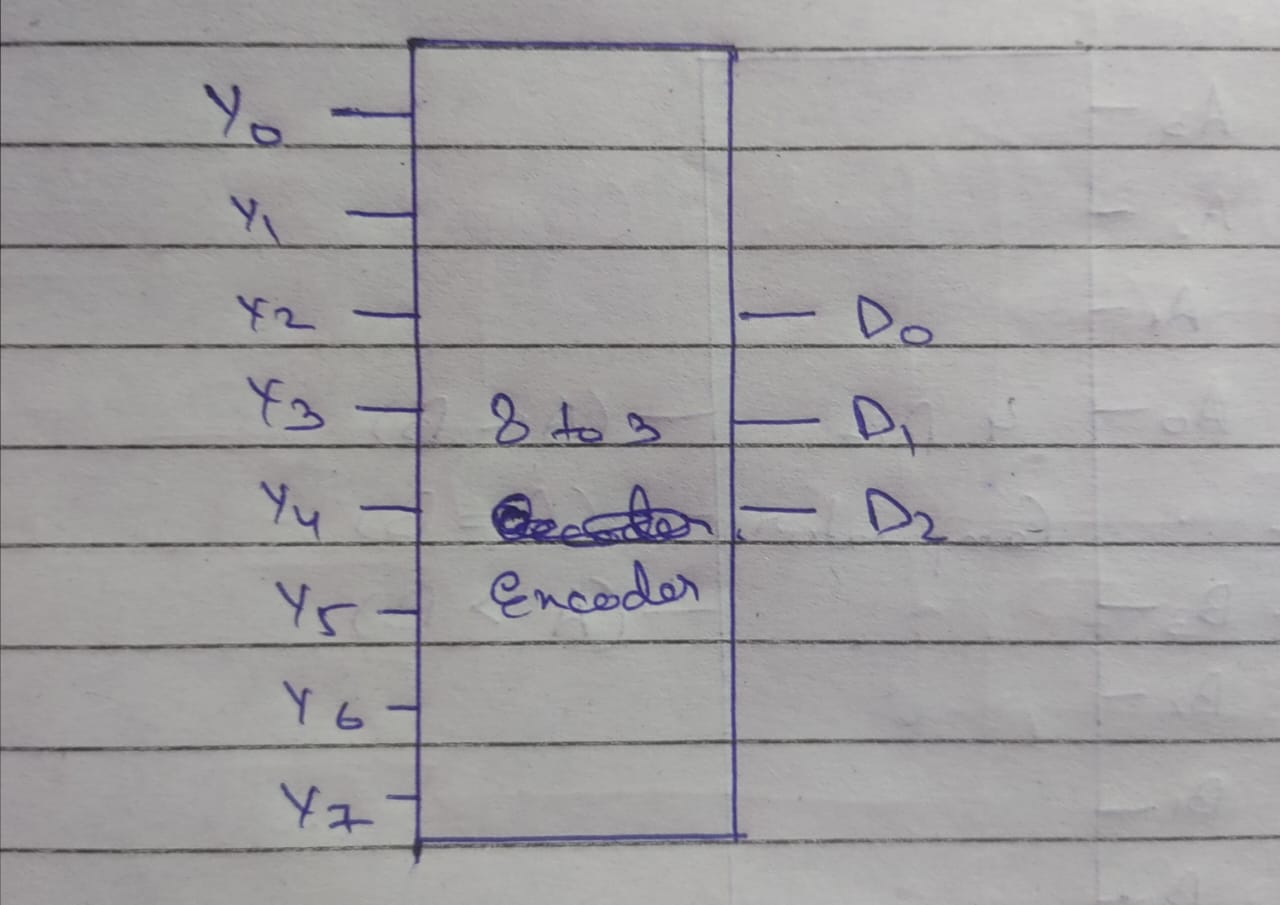


**Question 3**

**Design a VHDL Model for an Octal to Binary Encoder with 8 input Bits and three output bits. Each input Bit represents one Octal number.**

**Aim : To design a VHDL model for an Octal-to-Binary Encoder with 8 input bits and 3 output bits, where each input bit represents an octal number.**

**Block Diagram :**



***● VHDL Code:***

***----------------------------------------------------------------------------------***

***-- Company:***

***-- Engineer:***

***--***

***-- Create Date: 20:16:54 09/22/2024***

***-- Design Name:***

***-- Module Name: octal\_to\_binary - Behavioral***

***-- Project Name:***

***-- Target Devices:***

***-- Tool versions:***

***-- Description:***

***--***

***-- Dependencies:***

***--***

***-- Revision:***

***-- Revision 0.01 - File Created***

***-- Additional Comments:***

***--***

***----------------------------------------------------------------------------------***

***library IEEE;***

***use IEEE.STD\_LOGIC\_1164.ALL;***

***-- Uncomment the following library declaration if using***

***-- arithmetic functions with Signed or Unsigned values***

***--use IEEE.NUMERIC\_STD.ALL;***

***-- Uncomment the following library declaration if instantiating***

***-- any Xilinx primitives in this code.***

***--library UNISIM;***

***--use UNISIM.VComponents.all;***

***entity octal\_to\_binary is***

***Port ( A : in STD\_LOGIC;***

***B : in STD\_LOGIC;***

***C : in STD\_LOGIC;***

***D : in STD\_LOGIC;***

***E : in STD\_LOGIC;***

***F : in STD\_LOGIC;***

***G : in STD\_LOGIC;***

***H : in STD\_LOGIC;***

***EN : in STD\_LOGIC;***

***Y0 : out STD\_LOGIC;***

***Y1 : out STD\_LOGIC;***

***Y2 : out STD\_LOGIC);***

***end octal\_to\_binary;***

***architecture Behavioral of octal\_to\_binary is***

***begin***

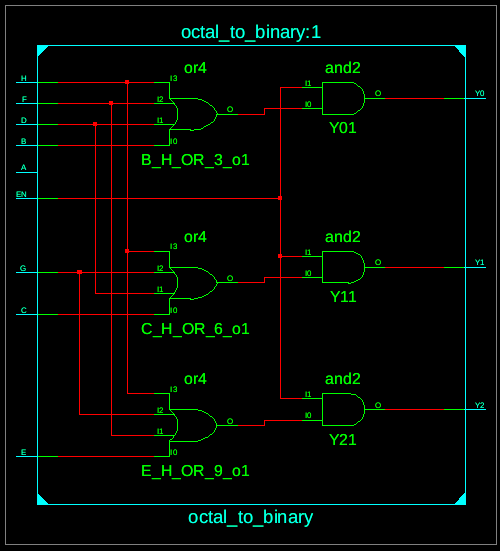
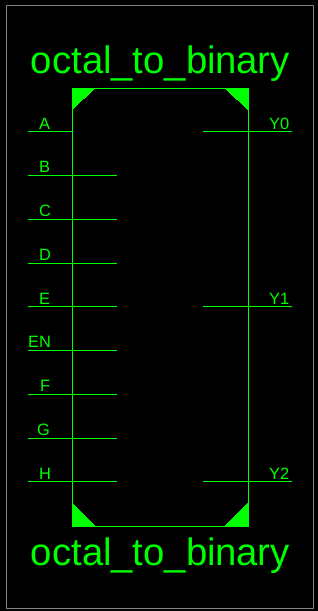
***Y0<=(B OR D OR F OR H )AND EN;***

***Y1<= (C OR D OR G OR H) AND EN;***

***Y2 <= (E OR F OR G OR H) AND EN;***

***end Behavioral;***

***● RTL Diagram:***



***● Testbench Code:   
--------------------------------------------------------------------------------***

***-- Company:***

***-- Engineer:***

***--***

***-- Create Date: 20:21:55 09/22/2024***

***-- Design Name:***

***-- Module Name: /home/ise/Assignment2/tb\_octal\_to\_binary.vhd***

***-- Project Name: Assignment2***

***-- Target Device:***

***-- Tool versions:***

***-- Description:***

***--***

***-- VHDL Test Bench Created by ISE for module: octal\_to\_binary***

***--***

***-- Dependencies:***

***--***

***-- Revision:***

***-- Revision 0.01 - File Created***

***-- Additional Comments:***

***--***

***-- Notes:***

***-- This testbench has been automatically generated using types std\_logic and***

***-- std\_logic\_vector for the ports of the unit under test. Xilinx recommends***

***-- that these types always be used for the top-level I/O of a design in order***

***-- to guarantee that the testbench will bind correctly to the post-implementation***

***-- simulation model.***

***--------------------------------------------------------------------------------***

***LIBRARY ieee;***

***USE ieee.std\_logic\_1164.ALL;***

***-- Uncomment the following library declaration if using***

***-- arithmetic functions with Signed or Unsigned values***

***--USE ieee.numeric\_std.ALL;***

***ENTITY tb\_octal\_to\_binary IS***

***END tb\_octal\_to\_binary;***

***ARCHITECTURE behavior OF tb\_octal\_to\_binary IS***

***-- Component Declaration for the Unit Under Test (UUT)***

***COMPONENT octal\_to\_binary***

***PORT(***

***A : IN std\_logic;***

***B : IN std\_logic;***

***C : IN std\_logic;***

***D : IN std\_logic;***

***E : IN std\_logic;***

***F : IN std\_logic;***

***G : IN std\_logic;***

***H : IN std\_logic;***

***EN : IN std\_logic;***

***Y0 : OUT std\_logic;***

***Y1 : OUT std\_logic;***

***Y2 : OUT std\_logic***

***);***

***END COMPONENT;***

***--Inputs***

***signal A : std\_logic := '0';***

***signal B : std\_logic := '0';***

***signal C : std\_logic := '0';***

***signal D : std\_logic := '0';***

***signal E : std\_logic := '0';***

***signal F : std\_logic := '0';***

***signal G : std\_logic := '0';***

***signal H : std\_logic := '0';***

***signal EN : std\_logic := '0';***

***--Outputs***

***signal Y0 : std\_logic;***

***signal Y1 : std\_logic;***

***signal Y2 : std\_logic;***

***-- No clocks detected in port list. Replace <clock> below with***

***-- appropriate port name***

***BEGIN***

***-- Instantiate the Unit Under Test (UUT)***

***uut: octal\_to\_binary PORT MAP (***

***A => A,***

***B => B,***

***C => C,***

***D => D,***

***E => E,***

***F => F,***

***G => G,***

***H => H,***

***EN => EN,***

***Y0 => Y0,***

***Y1 => Y1,***

***Y2 => Y2***

***);***

***-- Stimulus process***

***stim\_proc: process***

***begin***

***A <= '0'; B <= '0'; C <= '0'; D <= '0'; E <= '1'; F <= '1'; G <= '0'; H <= '0';***

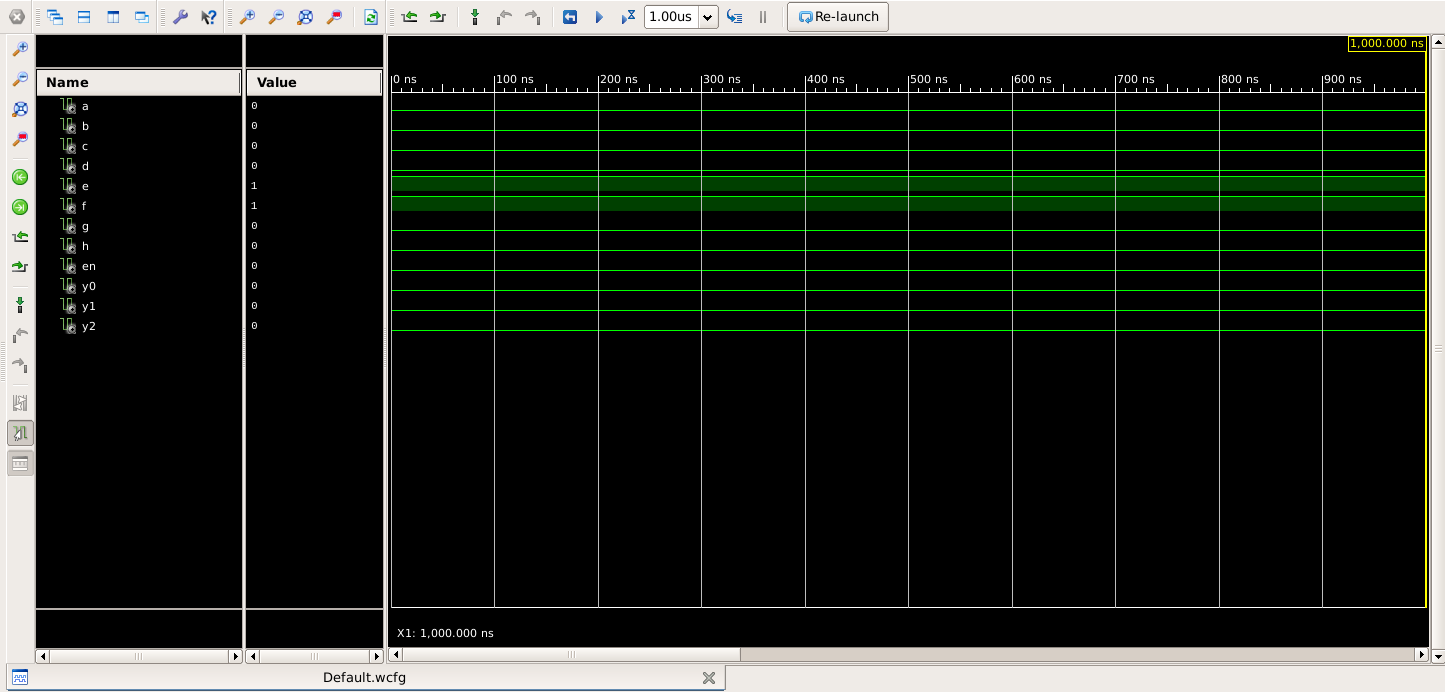
***wait for 10 ns;***

***wait;***

***end process;***

***END;***

***● Waveform:***

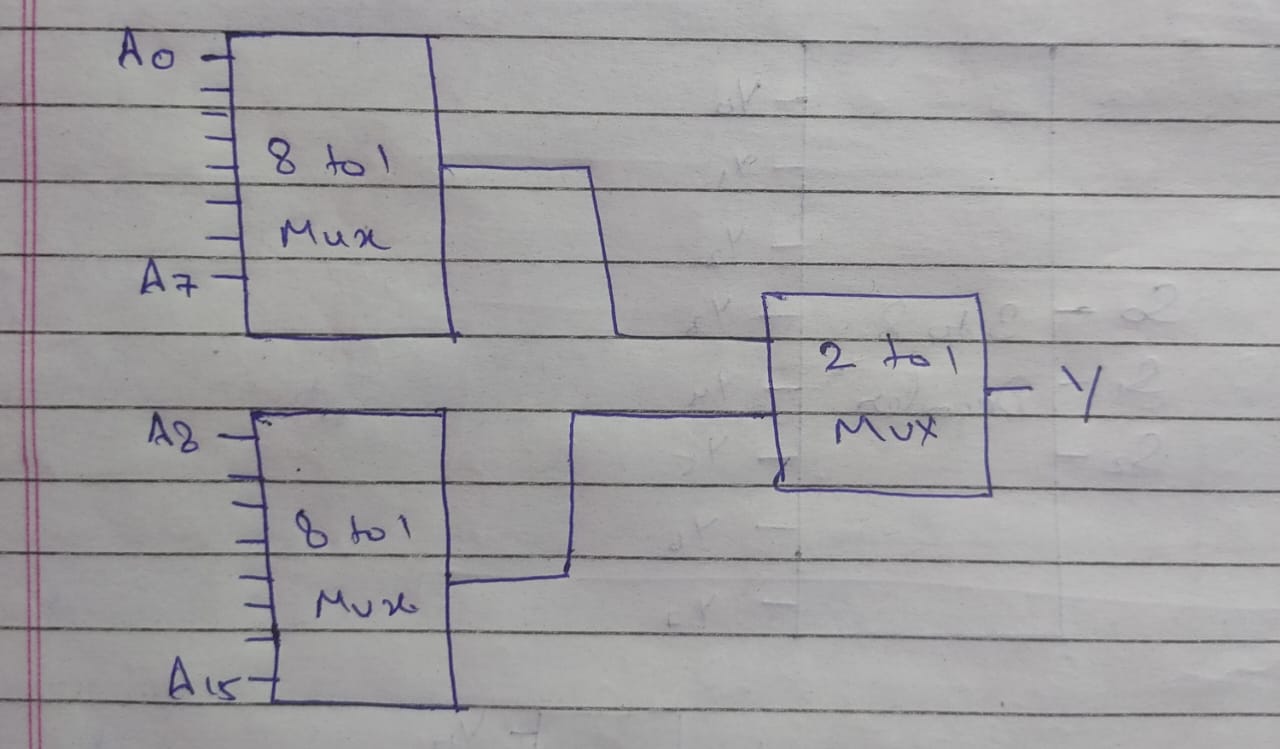


**Question 4**

**Design a VHDL model for 8-1 and 2-1 multiplexer. Using these models develop a VHDL model for 16 -1 multiplexer (Use structural architecture).**

**Aim : To design VHDL models for an 8-to-1 multiplexer (MUX) and a 2-to-1 multiplexer, and use these models to develop a 16-to-1 multiplexer using Structural Architecture.**

**Block Diagram :**



**8 To 1 Multiplexer:**

***● VHDL Code:***

***----------------------------------------------------------------------------------***

***-- Company:***

***-- Engineer:***

***--***

***-- Create Date: 20:26:12 09/22/2024***

***-- Design Name:***

***-- Module Name: mux\_8\_to\_1 - Behavioral***

***-- Project Name:***

***-- Target Devices:***

***-- Tool versions:***

***-- Description:***

***--***

***-- Dependencies:***

***--***

***-- Revision:***

***-- Revision 0.01 - File Created***

***-- Additional Comments:***

***--***

***----------------------------------------------------------------------------------***

***library IEEE;***

***use IEEE.STD\_LOGIC\_1164.ALL;***

***-- Uncomment the following library declaration if using***

***-- arithmetic functions with Signed or Unsigned values***

***--use IEEE.NUMERIC\_STD.ALL;***

***-- Uncomment the following library declaration if instantiating***

***-- any Xilinx primitives in this code.***

***--library UNISIM;***

***--use UNISIM.VComponents.all;***

***entity mux\_8\_to\_1 is***

***Port ( A : in STD\_LOGIC\_VECTOR (7 downto 0);***

***S1,S2,S3: IN STD\_LOGIC;***

***Y : out STD\_LOGIC);***

***end mux\_8\_to\_1;***

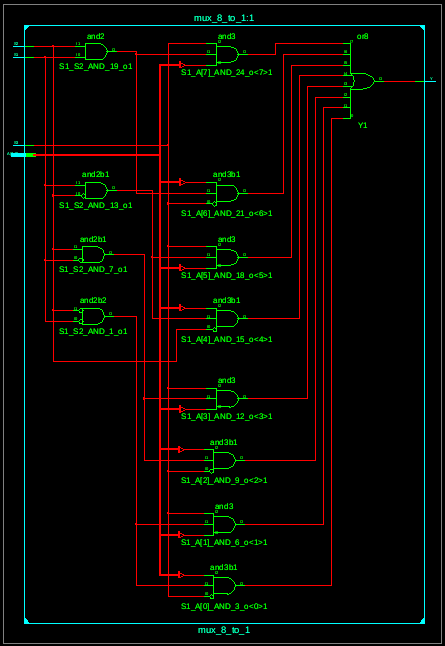
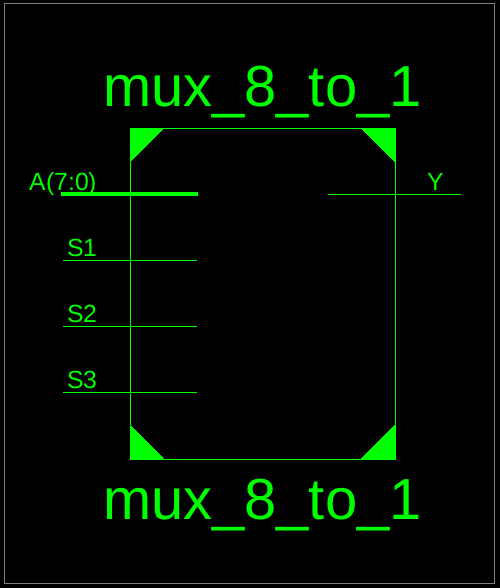
***architecture Behavioral of mux\_8\_to\_1 is***

***begin***

***Y<=((NOT (S1) AND NOT(S2) AND NOT (S3) AND A(0)) OR (NOT (S1) AND NOT (S2) AND S3 AND A(1)) OR (NOT(S1) AND S2 AND NOT(S3) AND A(2)) OR (NOT (S1) AND S2 AND S3 AND A(3)) OR (S1 AND NOT(S2) AND NOT(S2) AND A(4)) OR (S1 AND NOT (S2) AND S3 AND A(5)) OR (S1 AND S2 AND NOT(S3) AND A(6)) OR(S1 AND S2 AND S3 AND A(7)));***

***end Behavioral;***

***● RTL Diagram:***



***● Testbench Code:   
--------------------------------------------------------------------------------***

***-- Company:***

***-- Engineer:***

***--***

***-- Create Date: 20:38:44 09/22/2024***

***-- Design Name:***

***-- Module Name: /home/ise/Assignment2/tb\_mux\_8\_to\_1.vhd***

***-- Project Name: Assignment2***

***-- Target Device:***

***-- Tool versions:***

***-- Description:***

***--***

***-- VHDL Test Bench Created by ISE for module: mux\_8\_to\_1***

***--***

***-- Dependencies:***

***--***

***-- Revision:***

***-- Revision 0.01 - File Created***

***-- Additional Comments:***

***--***

***-- Notes:***

***-- This testbench has been automatically generated using types std\_logic and***

***-- std\_logic\_vector for the ports of the unit under test. Xilinx recommends***

***-- that these types always be used for the top-level I/O of a design in order***

***-- to guarantee that the testbench will bind correctly to the post-implementation***

***-- simulation model.***

***--------------------------------------------------------------------------------***

***LIBRARY ieee;***

***USE ieee.std\_logic\_1164.ALL;***

***-- Uncomment the following library declaration if using***

***-- arithmetic functions with Signed or Unsigned values***

***--USE ieee.numeric\_std.ALL;***

***ENTITY tb\_mux\_8\_to\_1 IS***

***END tb\_mux\_8\_to\_1;***

***ARCHITECTURE behavior OF tb\_mux\_8\_to\_1 IS***

***-- Component Declaration for the Unit Under Test (UUT)***

***COMPONENT mux\_8\_to\_1***

***PORT(***

***A : IN std\_logic\_vector(7 downto 0);***

***S1 : IN std\_logic;***

***S2 : IN std\_logic;***

***S3 : IN std\_logic;***

***Y : OUT std\_logic***

***);***

***END COMPONENT;***

***--Inputs***

***signal A : std\_logic\_vector(7 downto 0) := (others => '0');***

***signal S1 : std\_logic := '0';***

***signal S2 : std\_logic := '0';***

***signal S3 : std\_logic := '0';***

***--Outputs***

***signal Y : std\_logic;***

***-- No clocks detected in port list. Replace <clock> below with***

***-- appropriate port name***

***BEGIN***

***-- Instantiate the Unit Under Test (UUT)***

***uut: mux\_8\_to\_1 PORT MAP (***

***A => A,***

***S1 => S1,***

***S2 => S2,***

***S3 => S3,***

***Y => Y***

***);***

***-- Stimulus process***

***stim\_proc: process***

***begin***

***A<="00101110";***

***S1<='1';S2<='1';S3<='1';***

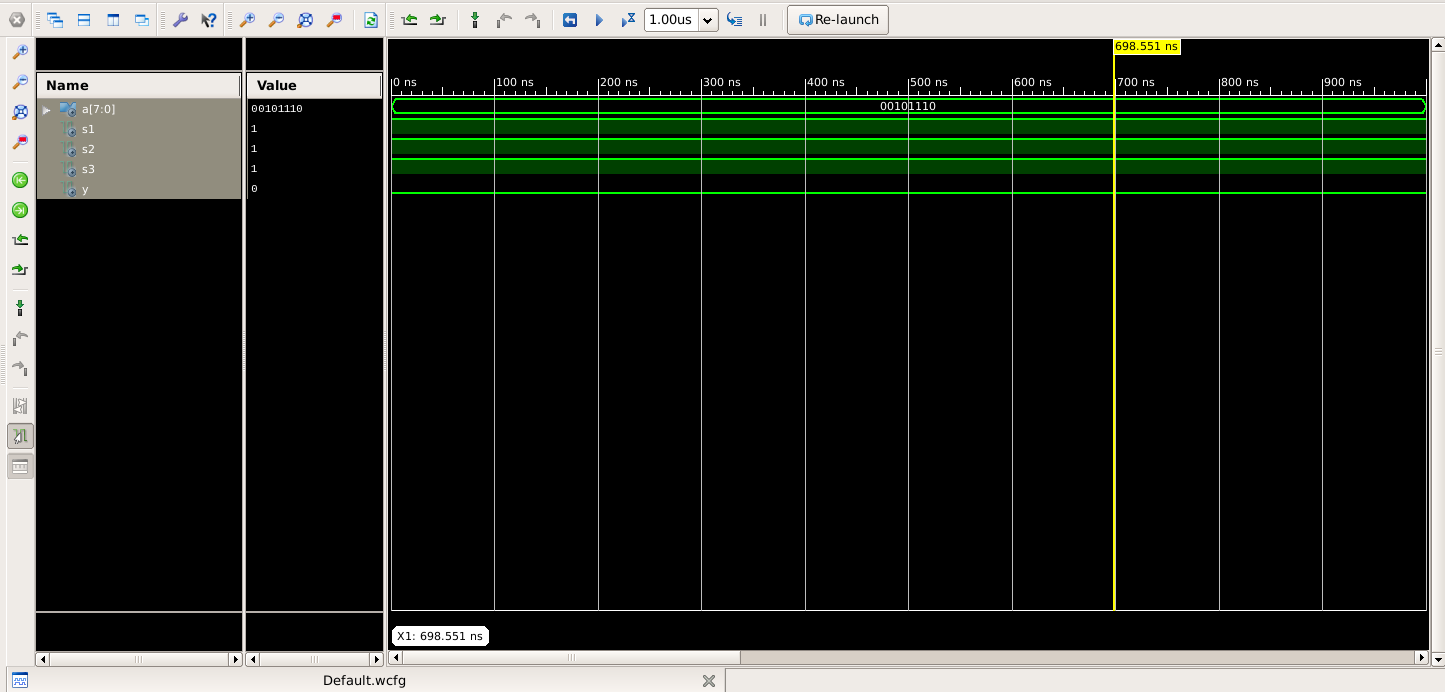
***wait for 100 ns;***

***wait;***

***end process;***

***END;***

***● Waveform:***



**2 To 1 Multiplexer:**

***● VHDL Code:***

***----------------------------------------------------------------------------------***

***-- Company:***

***-- Engineer:***

***--***

***-- Create Date: 20:42:59 09/22/2024***

***-- Design Name:***

***-- Module Name: mux\_2\_to\_1 - Behavioral***

***-- Project Name:***

***-- Target Devices:***

***-- Tool versions:***

***-- Description:***

***--***

***-- Dependencies:***

***--***

***-- Revision:***

***-- Revision 0.01 - File Created***

***-- Additional Comments:***

***--***

***----------------------------------------------------------------------------------***

***library IEEE;***

***use IEEE.STD\_LOGIC\_1164.ALL;***

***-- Uncomment the following library declaration if using***

***-- arithmetic functions with Signed or Unsigned values***

***--use IEEE.NUMERIC\_STD.ALL;***

***-- Uncomment the following library declaration if instantiating***

***-- any Xilinx primitives in this code.***

***--library UNISIM;***

***--use UNISIM.VComponents.all;***

***entity mux\_2\_to\_1 is***

***Port ( A : in STD\_LOGIC;***

***B : in STD\_LOGIC;***

***S1 : in STD\_LOGIC;***

***Y : out STD\_LOGIC);***

***end mux\_2\_to\_1;***

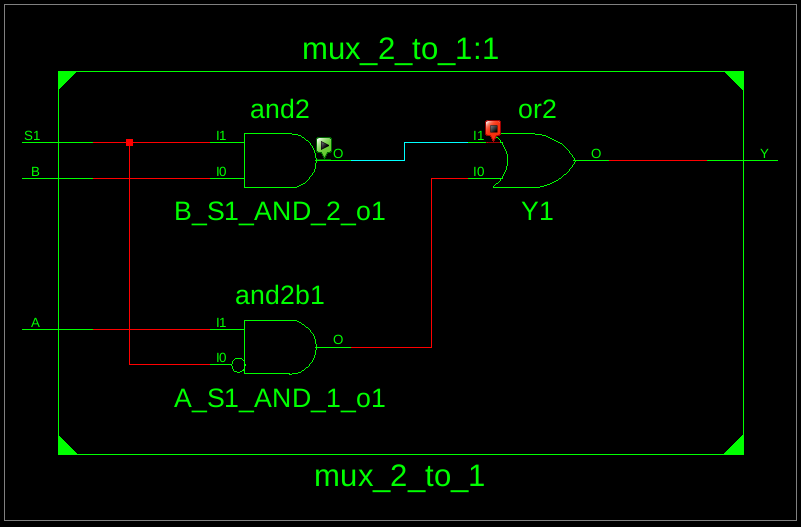
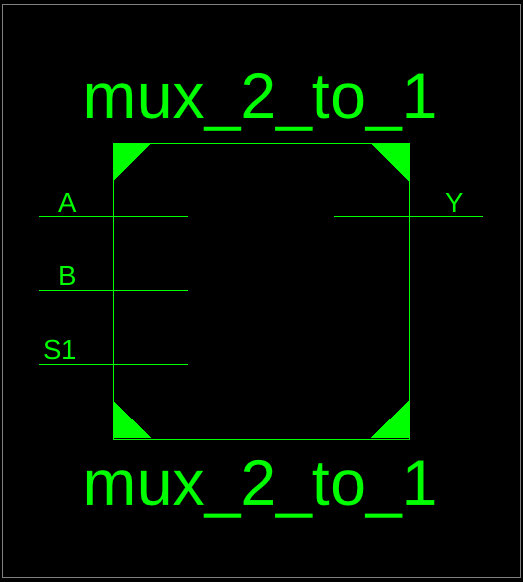
***architecture Behavioral of mux\_2\_to\_1 is***

***begin***

***Y<=(A AND NOT(S1)) OR (B AND S1);***

***end Behavioral;***

***● RTL Diagram:***



***● Testbench Code:   
--------------------------------------------------------------------------------***

***-- Company:***

***-- Engineer:***

***--***

***-- Create Date: 20:45:40 09/22/2024***

***-- Design Name:***

***-- Module Name: /home/ise/Assignment2/tb\_mux\_2\_to\_1.vhd***

***-- Project Name: Assignment2***

***-- Target Device:***

***-- Tool versions:***

***-- Description:***

***--***

***-- VHDL Test Bench Created by ISE for module: mux\_2\_to\_1***

***--***

***-- Dependencies:***

***--***

***-- Revision:***

***-- Revision 0.01 - File Created***

***-- Additional Comments:***

***--***

***-- Notes:***

***-- This testbench has been automatically generated using types std\_logic and***

***-- std\_logic\_vector for the ports of the unit under test. Xilinx recommends***

***-- that these types always be used for the top-level I/O of a design in order***

***-- to guarantee that the testbench will bind correctly to the post-implementation***

***-- simulation model.***

***--------------------------------------------------------------------------------***

***LIBRARY ieee;***

***USE ieee.std\_logic\_1164.ALL;***

***-- Uncomment the following library declaration if using***

***-- arithmetic functions with Signed or Unsigned values***

***--USE ieee.numeric\_std.ALL;***

***ENTITY tb\_mux\_2\_to\_1 IS***

***END tb\_mux\_2\_to\_1;***

***ARCHITECTURE behavior OF tb\_mux\_2\_to\_1 IS***

***-- Component Declaration for the Unit Under Test (UUT)***

***COMPONENT mux\_2\_to\_1***

***PORT(***

***A : IN std\_logic;***

***B : IN std\_logic;***

***S1 : IN std\_logic;***

***Y : OUT std\_logic***

***);***

***END COMPONENT;***

***--Inputs***

***signal A : std\_logic := '0';***

***signal B : std\_logic := '0';***

***signal S1 : std\_logic := '0';***

***--Outputs***

***signal Y : std\_logic;***

***-- No clocks detected in port list. Replace <clock> below with***

***-- appropriate port name***

***BEGIN***

***-- Instantiate the Unit Under Test (UUT)***

***uut: mux\_2\_to\_1 PORT MAP (***

***A => A,***

***B => B,***

***S1 => S1,***

***Y => Y***

***);***

***-- Stimulus process***

***stim\_proc: process***

***begin***

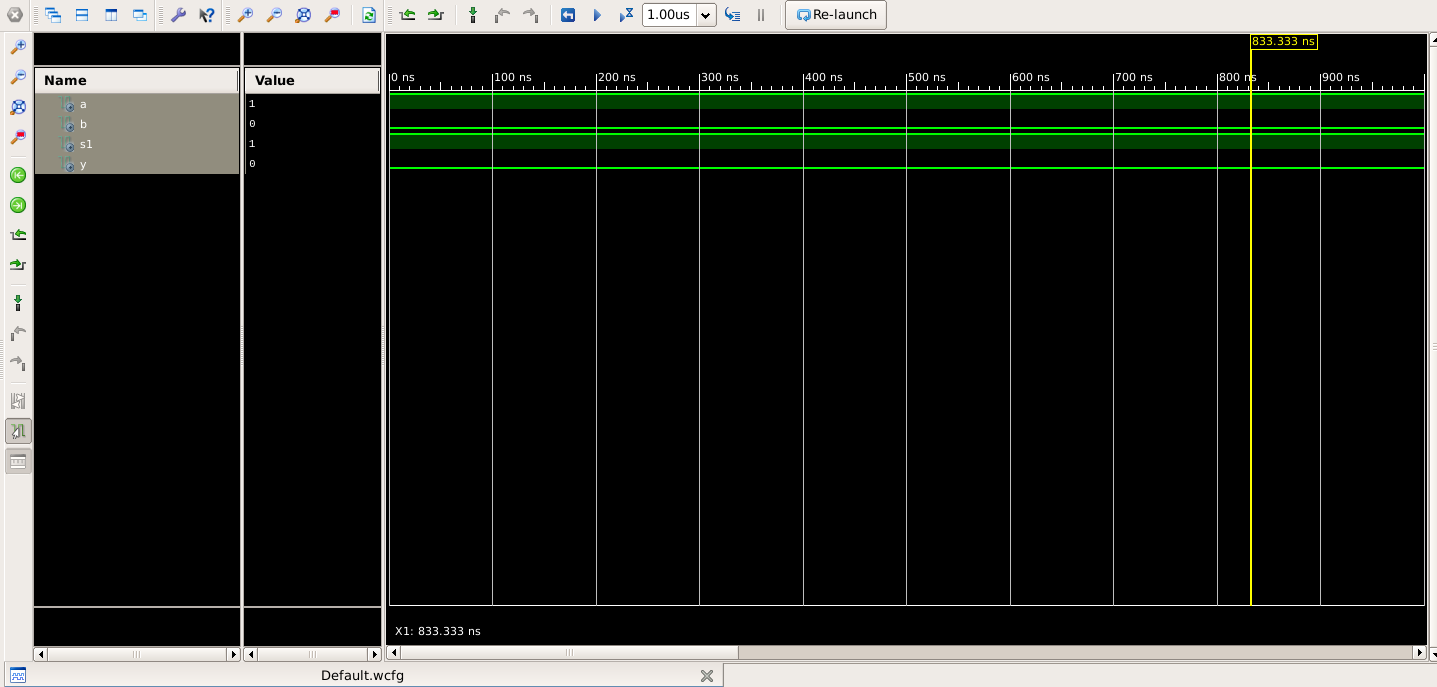
***A<='1';B<='0';S1<='1';***

***wait;***

***end process;***

***END;***

***● Waveform:***



**16 To 1 Multiplexer:**

***● VHDL Code:***

***----------------------------------------------------------------------------------***

***-- Company:***

***-- Engineer:***

***--***

***-- Create Date: 20:50:00 09/22/2024***

***-- Design Name:***

***-- Module Name: mux\_16\_to\_1 - Behavioral***

***-- Project Name:***

***-- Target Devices:***

***-- Tool versions:***

***-- Description:***

***--***

***-- Dependencies:***

***--***

***-- Revision:***

***-- Revision 0.01 - File Created***

***-- Additional Comments:***

***--***

***----------------------------------------------------------------------------------***

***library IEEE;***

***use IEEE.STD\_LOGIC\_1164.ALL;***

***-- Uncomment the following library declaration if using***

***-- arithmetic functions with Signed or Unsigned values***

***--use IEEE.NUMERIC\_STD.ALL;***

***-- Uncomment the following library declaration if instantiating***

***-- any Xilinx primitives in this code.***

***--library UNISIM;***

***--use UNISIM.VComponents.all;***

***entity mux\_16\_to\_1 is***

***Port ( A : in STD\_LOGIC\_VECTOR (15 downto 0);***

***S : in STD\_LOGIC\_VECTOR (3 downto 0);***

***Y : out STD\_LOGIC);***

***end mux\_16\_to\_1;***

***architecture Behavioral of mux\_16\_to\_1 is***

***component mux\_8\_to\_1 is***

***Port (***

***A : in STD\_LOGIC\_VECTOR (7 downto 0);***

***S1,S2,S3: IN STD\_LOGIC;***

***Y : out STD\_LOGIC);***

***end component;***

***component mux\_2\_to\_1 is***

***Port (***

***A : in STD\_LOGIC;***

***B : in STD\_LOGIC;***

***S1 : in STD\_LOGIC;***

***Y : out STD\_LOGIC);***

***end component;***

***signal t1,t2:std\_logic;***

***begin***

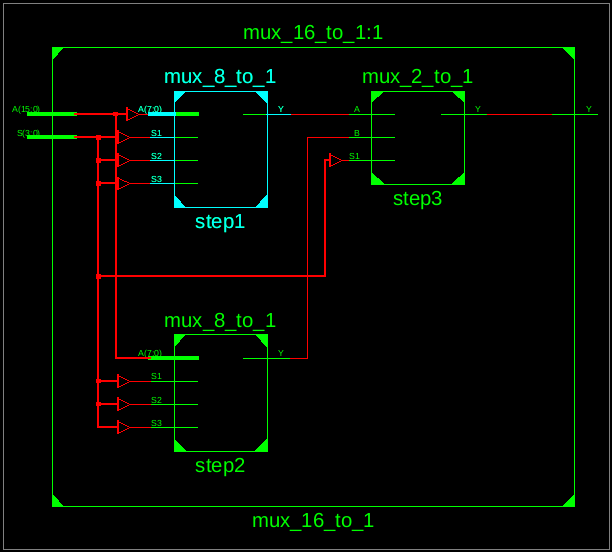
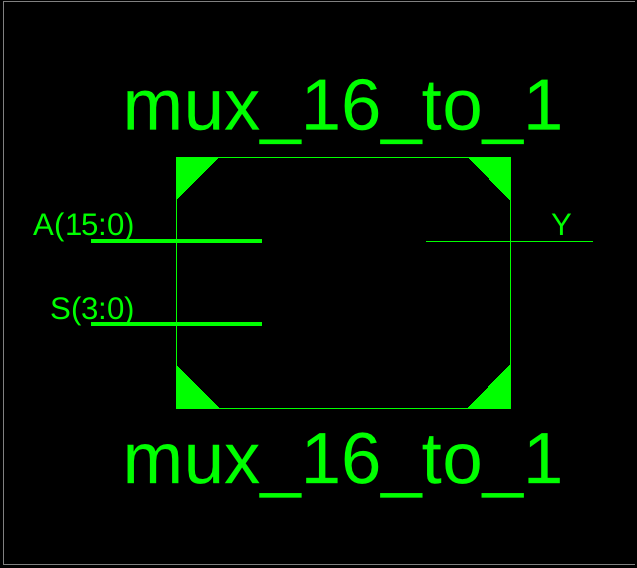
***step1:mux\_8\_to\_1 port map (A=>A(7 DOWNTO 0),S1=>S(0),S2=>S(1),S3=>S(2),Y=>t1);***

***step2:mux\_8\_to\_1 port map (A=>A(15 DOWNTO 8),S1=>S(0),S2=>S(1),S3=>S(2),Y=>t2);***

***step3:mux\_2\_to\_1 port map(A=>t1,B=>t2,S1=>S(3),Y=>Y);***

***end Behavioral;***

***● RTL Diagram:***



***● Testbench Code:   
--------------------------------------------------------------------------------***

***-- Company:***

***-- Engineer:***

***--***

***-- Create Date: 20:58:19 09/22/2024***

***-- Design Name:***

***-- Module Name: /home/ise/Assignment2/tb\_mux\_16\_to\_1.vhd***

***-- Project Name: Assignment2***

***-- Target Device:***

***-- Tool versions:***

***-- Description:***

***--***

***-- VHDL Test Bench Created by ISE for module: mux\_16\_to\_1***

***--***

***-- Dependencies:***

***--***

***-- Revision:***

***-- Revision 0.01 - File Created***

***-- Additional Comments:***

***--***

***-- Notes:***

***-- This testbench has been automatically generated using types std\_logic and***

***-- std\_logic\_vector for the ports of the unit under test. Xilinx recommends***

***-- that these types always be used for the top-level I/O of a design in order***

***-- to guarantee that the testbench will bind correctly to the post-implementation***

***-- simulation model.***

***--------------------------------------------------------------------------------***

***LIBRARY ieee;***

***USE ieee.std\_logic\_1164.ALL;***

***-- Uncomment the following library declaration if using***

***-- arithmetic functions with Signed or Unsigned values***

***--USE ieee.numeric\_std.ALL;***

***ENTITY tb\_mux\_16\_to\_1 IS***

***END tb\_mux\_16\_to\_1;***

***ARCHITECTURE behavior OF tb\_mux\_16\_to\_1 IS***

***-- Component Declaration for the Unit Under Test (UUT)***

***COMPONENT mux\_16\_to\_1***

***PORT(***

***A : IN std\_logic\_vector(15 downto 0);***

***S : IN std\_logic\_vector(3 downto 0);***

***Y : OUT std\_logic***

***);***

***END COMPONENT;***

***--Inputs***

***signal A : std\_logic\_vector(15 downto 0) := (others => '0');***

***signal S : std\_logic\_vector(3 downto 0) := (others => '0');***

***--Outputs***

***signal Y : std\_logic;***

***-- No clocks detected in port list. Replace <clock> below with***

***-- appropriate port name***

***BEGIN***

***-- Instantiate the Unit Under Test (UUT)***

***uut: mux\_16\_to\_1 PORT MAP (***

***A => A,***

***S => S,***

***Y => Y***

***);***

***-- Stimulus process***

***stim\_proc: process***

***begin***

***A<="1000000010000000";***

***S<="1111";***

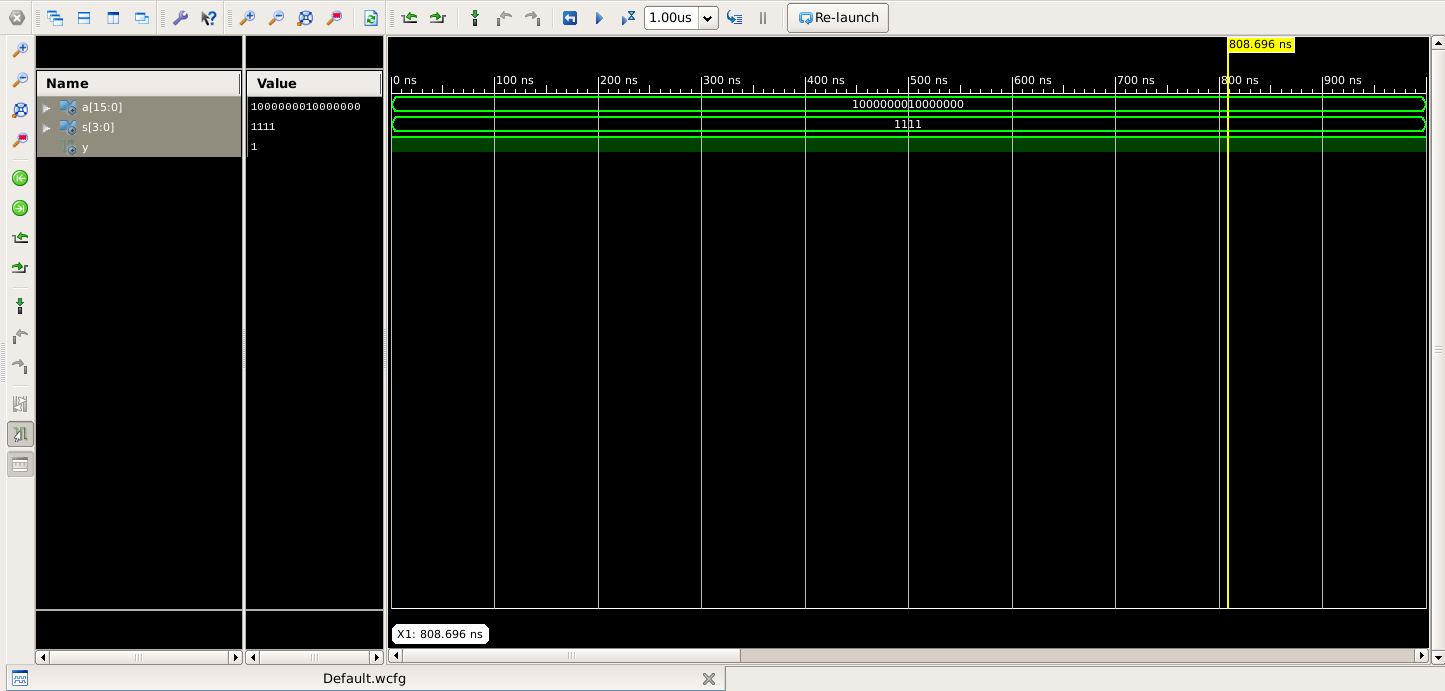
***wait for 100 ns;***

***wait;***

***end process;***

***END;***

***● Waveform:***



Proof That it Was Not Copied

***You can check My Github Account***

<https://github.com/ij-roy/Semester-3/tree/main/COA/Assignment%202>

***I had uploaded Every picture and code used above and you can also check the Date of Upload***

**Thank You**